
SpartanMC

***Configurable Parallel Input for 1
to 18 Bit (port_in)***

Table of Contents

1. Module Parameters	1
2. Interrupts	1
3. Peripheral Registers	1
3.1. Input Port Register Description	1
3.2. PORT_IN C-Header for Register Description	2

List of Figures

List of Tables

0 PORT_IN module parameters	1
0 PORT_IN registers	1

Configurable Parallel Input for 1 to 18 Bit (port_in)

The input port module provides up to 18 input signals. These inputs can be used for switches, buttons etc.. Furthermore, they can be configured to generate interrupts (triggered by a raising or falling edge) as SoC input. Each input pin provides separate configuration bits.

1. Module Parameters

Table 1: PORT_IN module parameters

Parameter	Default Value	Description
BASE_ADR		Start address of the memory mapped peripheral registers. The value is taken as offset to the start address of the peripheral memory space. This parameter is set by jConfig automatically.
PORT_WIDTH	18	Number of input bits.

2. Interrupts

An interrupt signal will be generated for each enabled PORT_IN bit. To delete the interrupt flag a read access on PIN_IN_DAT, PIN_IN_IE or PIN_IN_EDGSEL is required.

3. Peripheral Registers

3.1. Input Port Register Description

The input port peripheral provides four 18 bit registers which are mapped to the SpartanMC address space e.g. $0x1A000 + \text{BASE_ADR} + \text{Offset}$.

Table 2: PORT_IN registers

Offset	Name	Access	Description
0	PIN_IN_DAT	read	Register for incoming data.

Offset	Name	Access	Description
1	PIN_IN_IE	read/ write	Enables the interrupts on PIN_IN_DAT register. After system reset all PIN_IN_IE bits are initialized with zero.
2	PIN_IN_EDGSEL	read/ write	Specify the input edge which triggers the interrupt (0 = falling edge, 1 = raising edge) After system reset all PIN_IN_EDGSEL bits are initialized with zero.
3	PIN_IN_IR_STATUS	read	Register for interrupt flags. If set to one it indicates an interrupt on the corresponding input pin. The interrupt flag will be deleted with a read access on all other module registers except this one. After system reset all PIN_IN_IR_STATUS bits are initialized with zero.

3.2. PORT_IN C-Header for Register Description

```
#ifndef PORT_IN_H_
#define PORT_IN_H_

#define IN00 (1 << 0)
#define IN01 (1 << 1)
#define IN02 (1 << 2)
#define IN03 (1 << 3)
#define IN04 (1 << 4)
#define IN05 (1 << 5)
#define IN06 (1 << 6)
#define IN07 (1 << 7)
#define IN08 (1 << 8)
#define IN09 (1 << 9)
#define IN10 (1 << 10)
#define IN11 (1 << 11)
#define IN12 (1 << 12)
#define IN13 (1 << 13)
#define IN14 (1 << 14)
#define IN15 (1 << 15)
#define IN16 (1 << 16)
#define IN17 (1 << 17)

typedef struct port_in {
    volatile unsigned int data; // (r) (r = reset-int)
    volatile unsigned int ie; // (r/w) (r = reset-int)
    volatile unsigned int edgsel; // (r/w) (r = reset-int)
    volatile unsigned int ir_stat; // (r)
} port_in_t;

#endif /*PORT_IN_H_*/
```